

TRANSMITTAL OF INFORMATION DISCLOSURE STATEMENT(Under 37 CFR 1.97(b) ~~and 1.97(e)~~)

Docket No.

13392

In Re Application Of: Koichi TAMURA

AUG 0 6 2001

Serial No.

09/510,861

Filing Date

2/23/2000

Examiner

Unassigned

Group Art Unit

2734

Title: **DEMODULATION AND MODULATION CIRCUIT AND DEMODULATION
AND MODULATION METHOD**

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Address to:

Assistant Commissioner for Patents
Washington, D.C. 20231

Technology Center 2600

37 CFR 1.97(b)

1. ☒ The Information Disclosure Statement submitted herewith is being filed within three months of the filing of a national application; within three months of the date of entry of the national stage as set forth in 37 CFR 1.491 in an international application; or before the mailing date of a first Office Action on the merits, whichever event occurs last.

37 CFR 1.97(c)

2. ☐ The Information Disclosure Statement submitted herewith is being filed after three months of the filing of a national application, or the date of entry of the national stage as set forth in 37 CFR 1.491 in an international application; or after the mailing date of a first Office Action on the merits, whichever occurred last but before the mailing date of either:

1. a Final Action under 37 CFR 1.113, or
2. a Notice of Allowance under 37 CFR 1.311,

whichever occurs first.

Also submitted herewith is:

- ☐ a certification as specified in 37 CFR 1.97(e);

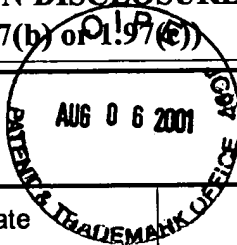
OR

- ☐ the fee set forth in 37 CFR 1.17(p) for submission of an Information Disclosure Statement under 37 CFR 1.97(c).

TRANSMITTAL OF INFORMATION DISCLOSURE STATEMENT
(Under 37 CFR 1.97(b) or 1.97(e))

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Payment of Fee

(Only complete if Applicant elects to pay the fee set forth in 37 CFR 1.17(p))

- ☐ A check in the amount of _____ is attached.
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Janet Grossman Typed or Printed Name of Person Mailing Correspondence	

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Dated: August 2, 2001

Signature
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(516) 742-4343

PJE:ae

CC:



6/8/9
PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant: Koichi TAMURA **Docket:** 13392
Serial No. 09/510,861 **Examiner:** Unassigned
Filed: February 23, 2000 **Group Art Unit:** 2734
For: DEMODULATION AND **Dated:** August 2, 2001
MODULATION CIRCUIT AND
DEMODULATION AND MODULATION
OF THE SAME

Assistant Commissioner for Patents
Washington, D.C. 20231

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INFORMATION DISCLOSURE STATEMENT

Sir:

In accordance with 37 C.F.R. §§1.97 and 1.98, it is requested that the following references, which are also listed on the attached Form PTO-1449, be made of record in the above-identified case.

1. Japanese Unexamined Patent Application No. 5-244144 dated September 21, 1993;
2. Japanese Unexamined Patent Application No. 8-139775 dated May 31, 1996;

CERTIFICATE OF MAILING UNDER 37 C.F.R. § 1.8(a)

I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail in an envelope addressed to: Assistant Commissioner for Patents, Washington, DC 20231 on. August 2, 2001.

Dated: August 2, 2001

Janet Grossman
Janet Grossman

3. Japanese Unexamined Patent Application No. 4-72932 dated March 6, 1992;
4. Japanese Unexamined Patent Application No. 8-242260 dated September 17, 1996;
5. Japanese Unexamined Patent Application No. 64-5135 dated January 10, 1989;
6. Japanese Unexamined Patent Application No. 8-88622 dated April 2, 1996;
7. Japanese Unexamined Patent Application No. 10-34163 dated December 22, 1998;
8. Japanese Unexamined Patent Application No. 8-307474 dated November 22, 1996;
9. Japanese Unexamined Patent Application No. 7-297870 dated November 10, 1995;
10. Japanese Unexamined Patent Application No. 11-103326 dated April 13, 1999;
11. Japanese Unexamined Patent Application No. 7-99486 dated April 11, 1995; and
12. Japanese Unexamined Patent Application No. 48-30308 dated April 21, 1973.

The references were cited in an Official Action dated May 29, 2001 received from the Japanese Patent Office. Applicant is submitting copies of the above-cited references, along with a translation of the Examiner's comments regarding the references from the Official Action. References 2, 4, and 9 are not provided as they were previously submitted together with an Information Disclosure Statement dated May 9, 2001. The relevance of the references is described in the Official Action.

In compliance with the requirements of 37 C.F.R. §1.98(a)(3), as a concise statement of relevance, as it is presently understood by the individual designated in 35 U.S.C. §1.56(c) most knowledgeable about the content of the information, the undersigned attorney of record submits a translation of portions of an official action by a foreign examiner in which the references were cited. The relevance to the pending U.S. patent application is that the references

were cited in a foreign patent application on the same subject matter. However, no independent analysis of the references, the accuracy of the statement of the foreign examiner or the claims of the foreign application under the laws of that country or the United States relative to the subject matter claimed in the present application has been made; the present understanding of the contents thereof by the undersigned being based on the translation of the foreign examiner's comments submitted herewith.

Inasmuch as this Information Disclosure Statement is being submitted in accordance with the schedule set out in 37 C.F.R. § 1.97(b), no statement or fee is required.

Respectfully submitted,



Paul J. Esatto, Jr.
Registration No. 30,749

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PJE:ae

Form PTO-1449 (REV. 7-80)		U.S. DEPARTMENT OF COMMERCE PATENT AND TRADEMARK OFFICE		Atty. Docket No. 13392		Serial No. 09/510,861	
LIST OF PRIOR ART CITED BY APPLICANT (Use several sheets if necessary)				Applicant Koichi Tamura			
Filing Date: February 23, 2000				Group Unassigned			

PTO
AUG 0 6 2001
PATENT & TRADEMARK OFFICE

U.S. PATENT DOCUMENTS							
EXAMINER INITIAL*		DOCUMENT NUMBER	DATE	NAME	CLASS	SUBCLASS	FILING DATE (if appropriate)

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FOREIGN PATENT DOCUMENTS								
		DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUBCLASS	TRANSLATION	
							YES	NO
cf		5-244144	9/21/93	JAPAN	—	—		
cf		4-72932	3/6/92	JAPAN	—	—		
cf		64-5135	1/10/89	JAPAN	—	—		
cf		8-88622	4/2/96	JAPAN	—	—		
cf		10-34163263	12/22/98	JAPAN	—	—		
cf		8-307474	11/22/96	JAPAN	—	—		
cf		11-103326	4/13/99	JAPAN	—	—		
cf		7-99486	4/11/95	JAPAN	—	—		
cf		48-30308	4/21/73	JAPAN	—	—		

OTHER PRIOR ART (Including Author, Title, Date, Pertinent Pages, Etc.)		

EXAMINER <i>Choi M L</i>	DATE CONSIDERED <i>11/5/03</i>
--------------------------	--------------------------------

* EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609; draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.



Docket No. 13392

UNITED STATES PATENT AND TRADEMARK OFFICE

VERIFICATION OF A TRANSLATION

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I, Susan POTTS BA ACIS,
Director of RWS Group plc, of Europa House, Marsham Way, Gerrards Cross,
Buckinghamshire, hereby England declare that:

My name and post office address are as stated below;

That the translator responsible for the attached translation is knowledgeable in the English language and in the Japanese language, and that, to the best of RWS Group plc knowledge and belief, the English translation of the marked portion of the attached Japanese document is true and complete.

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

Date: June 22, 2001

Signature of the director:

For and on behalf of RWS Group plc

Post Office Address :

Europa House, Marsham Way,
Gerrards Cross, Buckinghamshire,
England.

The inventions pertaining to the following claims of the application cannot be granted patent rights in accordance with the provisions of Patent Act, Article 29, Section 2 because, based on the inventions disclosed in the publications itemized below which were circulated within and outside Japan before the application, they could have been easily invented prior to the application by a person having knowledge common to the field of technology to which the inventions belong.

ITEM

< List of Cited Documents >

1. Japanese Unexamined Patent Application No. Heisei 5-244144
2. Japanese Unexamined Patent Application No. Heisei 8-139775
3. Japanese Unexamined Patent Application No. Heisei 4-72932
4. Japanese Unexamined Patent Application No. Heisei 8-242260
5. Japanese Unexamined Patent Application No. Showa 64-5135
6. Japanese Unexamined Patent Application No. Heisei 8-88622

• Regarding Claim 1: Corresponding Cited Document 1

(Remarks)

Figure 1 and the specification of cited document 1 provided a description of a demodulated-dispatch which, in a demodulating device which, during transmission, receives and demodulates a transmitted signal in which a known signal has been inserted in advance, comprises an A/D converter (11) for converting a base-band signal, and a phase shift means (UW detector circuit 12 and timing generation circuit 14) which, based on the output signal of the A/D converter and the above-mentioned known signal, shifts the sampling timing in the above-mentioned A/D converter, wherein the invention described in this cited document is not regarded as especially different to the invention pertaining to claim 1 of the present application.

• Claim 2: Cited documents 1 - 2

(Remarks)

In a comparison of the invention pertaining to claim 2 of the present application and the invention described in cited document 1, the following points of difference are regarded as existing between the two:

(1) The point that, in contrast to the invention of the present application in which an "orthogonal demodulating means", two "A/D converters" and a "symbol judging part",

are provided, these are not provided in the invention of cited document 1; and

(2) The point that, in contrast to the invention of the present application in which a "phase shifter which shifts the phase of the base-band signal" is employed as a phase shift means for phase shifting the sampling timing in an A/D converter means, shifting of the phase of the sampling clock supplied to the A/D converter (11) is not performed in the invention described in cited document 1.

The adoption of the invention of the present application in a PSK demodulating device such as this (that is to say, the comparing of the data output by the symbol judgment part (data identifier 6, 7) in the PSK demodulating circuit described of cited document 2 and the shifting of the sampling timing of an A/D converter in response to the compared results) is regarded as one which, if the person was skilled in the art, would be simple to devise.

An examination of the above noted points of difference, described below, was carried out.

(1) As is described in Figure 1 of cited document 2, a PSK demodulating circuit which employs an orthogonal demodulating circuit (2 mixers provided in the pre-stage of the LPF 1, 2), which comprises two A/D converters, and which further employs a symbol judging part (data

identification part 6, 7), constitutes a well-known circuit.

(2) As the general means for converting the sampling timing in an A/D converter, whether the phase of a signal for sampling (that is to say, a base-band signal) is shifted, or, the phase of a sampling clock is converted, is regarded as, simply, a matter of design to be selected, as appropriate, and in accordance with need, by the person skilled in the art. As a result, the adoption of, as the means for phase shifting of the sampling timing in the A/D converter in the invention described in cited document 1, a means for converting the phase of a signal for sampling (that is to say, a base-band signal) rather than a means for converting the phase of the sampling clock, is regarded as simple for the person skilled in the art.

From the results of the above examination, the invention pertaining to claim 2 of the present application is, based on the invention described in cited document 1 and the well-known technology described in cited document 2, regarded as being able to be easily devised by a person skilled in the art.

• Claim 3: Cited documents 1, 2

(Remarks)

In a comparison of the invention pertaining to claim 1 of the present application and the invention described in cited document 3, the following points of difference are regarded as existing between the two:

- (1) The point that, in contrast to the invention of the present application in which a configuration is adopted which employs an "orthogonal demodulating means", "symbol judging part" and a "P/S converter", and which comprises two "A/D converters", the invention described in cited document 1 does not comprise such a configuration; and
- (2) The point that, in contrast to the invention of the present application in which a "phase shifter which shifts the phase of the base-band signal" is employed as a phase shift means for phase shifting the sampling timing in an A/D converter means, shifting of the phase of the sampling clock supplied to the A/D converter (11) is not performed in the invention described in cited document 1.

An examination of the above noted points of difference, described below, was carried out.

- (1) As is described in Figure 1 of cited document 2, the PSK demodulating circuit which comprises an orthogonal demodulating circuit, two A/D converters, a symbol judging part and a P/S converter part, constitutes a well-known device, and the application of the invention of the present application to a PSK demodulating device

such as this (that is to say, a configuration in which phase lag of the sampling timing in the A/D converter is detected and corrected by comparing demodulated data output by the P/S converter 15 in the demodulating circuit described in cited document 2 with the known signal of the invention described in cited document 1) can only be described as very simple.

(2) As the general means for converting the sampling timing in an A/D converter, whether the phase of a signal for sampling (that is to say, a base-band signal) is shifted, or, the phase of a sampling clock is converted, is regarded as, simply, a matter of design to be selected, as appropriate, and in accordance with need, by the person skilled in the art. As a result, the adoption of, as the means for phase shifting of the sampling timing in the A/D converter in the invention described in cited document 1, a means for converting the phase of a signal for sampling (that is to say, a base-band signal) rather than a means for converting the phase of the sampling clock, is regarded as simple for the person skilled in the art.

From the results of the above examination, the invention pertaining to claim 2 and claim 5 of the present application are, based on the invention described in cited document 1 and the well-known technology described in cited document 2, regarded as being able to be easily devised by a person skilled in the art.

• Claim 4: Cited documents 1, 2

(Remarks)

In the technology described in cited document 2, the provision of the some kind of data processing means in a post-stage of the P/S converter 15 is self-evident.

• Claim 5: Cited documents 1, 2

(Remarks)

In the demodulating circuit described in cited document 2, although a means for shifting the phase of the sampling clock is adopted as a means for shifting of the sampling timing in the A/D converter, designing of the conversion in such a way that the phase of the signal for sampling is shifted is, as described before, regarded as easy to devise for the person skilled in the art.

(See remarks regarding the invention pertaining to claim 3)

It is self-evident that, at this time, two base-band signals input in the A/D converters (3, 4), or a digital signal input in orthogonal demodulating means (two mixers), may be adopted as the "signals which are sampled" in the shifting of the phase.

Accordingly, the adoption of, as a means for shifting of the sampling timing in the A/D converter in the circuit described in cited document 2, a means for shifting the phase of the digital signal input in the

orthogonal demodulating means ("converted wave") rather than a means for shifting the phase of the sampling clock, is regarded as simple for the person skilled in the art.

Accordingly, the invention of claim 5 of the present application is, based on the inventions described in cited document 1 and 2, regarded as being able to be easily devised by a person skilled in the art.

• Claim 6, 7: Cited documents 1 - 3

(Remarks)

As is described in Figure 1 and the description of cited document 3, using a device for the comparison (see the operation of the correlating device 103) of a received data signal and a known signal (synchronized word pattern), the detection of the phase amount based on a plurality of compared results constitutes well-known technology (in cited document 3, detection is performed using the maximum value of the compared results within one frame).

The inventions pertaining to Claims 6 and 7 of the present application are, based on the inventions described in cited document 1 and the well known technology described in cited documents 2 and 3, regarded as being able to be easily devised by a person skilled in the art.

• Claim 8: Cited documents 1 - 4

(Remarks)

As is described in Figure 1 of cited document 4, the averaging of the detected phase amount ("Average/ $\Delta\theta$ corrected valued determining part 7") constitutes well-known technology.

• Claim 9: Cited documents 1 - 4

(Remarks)

The received signal in the invention described in cited document 1 constitutes a signal in which the information data and known signal have been time-multiplexed.

• Claim 10: Cited documents 1 - 5

(Remarks)

As is described in cited document 5, when two kinds of signal (in cited document 5, the "upper bit" and "lower bit") are to be transmitted, the technology for separately modulating and sending the orthogonal bi-axial carrier waves (I, Q), and the technology for receiving and demodulating the signal which has been sent in this way, constitutes well-known technology. (Please see, in particular, the description given in the section "Means to Solve the Problems" in the lower left column of page 2 of cited document 5).

The application of this well-known technology to be invention of cited document 1 is not regarded as special so, the invention of claim 10 of the present application is, based on the invention described in cited document 1 and the technology described in cited documents 2 to 5, regarded as being able to be easily devised by a person skilled in the art.

• Claim 11: Cited document 1

(Remarks)

Paragraph 2 of the text of cited document 1 describes a transmission circuit that is provided with a means for insertion of a known signal ("unique word") in a digital signal ("data signal").

The invention pertaining to claim 11 of the present application and the invention described in cited document 1 is not regarded as being especially different.

• Claim 12: Cited document 1

(Remarks)

The employment of an orthogonal modulator as a modulating means constitutes, without need to cite an example, well-known technology.

• Claim 13: Cited documents 1, 6

(Remarks)

The time multiplexing of a known signal and a digital signal constitutes, as described in Figure 1 of cited document 6, well-known technology (please see the operation of the signal conversion part 1 and the operation of the frame-pattern insertion part 10).

• Claim 14: Cited documents 1, 5

(Remarks)

Figure 2 of cited document 5 also describes technology in which, when two kinds of signal (in cited document 5, the "upper bit" and "lower bit") are to be transmitted, the orthogonal bi-axial carrier waves (I, Q) is separately modulated and sent using the abovementioned two kinds of signals.

The adoption, in the invention described in cited document 1 (paragraph 2 of the text), of the well-known technology described in cited document 5 as the specific modulating means, is not regarded as especially difficult.

• Claims 15 to 28: Cited documents 1 - 6

(Remarks)

The inventions pertaining to claims 15 to 28, in that only the category ("device of the invention" and "method of the invention") is different, are regarded as essentially comprising the same details as the inventions pertaining to each of the claims 1 to 14.

Accordingly, the inventions pertaining to claims 15 to 28 are, based on the well-known technology described in cited invention of cited document 1 and the well-known technology described in cited documents 2 to 6, in the same way as the inventions pertaining to claims 1 to 14, regarded as being able to be devised easily by a person skilled in the art.

Record of Results of the Prior Art Documents Search

• Field searched IPC Edition 7

H04L 27/00 - 27/38

H04L 7/00 - 7/10

• Prior Art Documents

Japanese Unexamined Patent Application No. Heisei

10-341263 (See the digital filter 8, 9 of Figure 1.

Reference document that corresponds to the digital filter 9, 10 of Figure 1 of the present application.)

Japanese Unexamined Patent Application No. Heisei

8-307474 (Description of technology in which a known signal is detected and, based on the detected results thereof, control of the sampling timing in the A/D converter is performed.)

Japanese Unexamined Patent Application No. Heisei 7-

297870 (Description of technology in which correlation is performed between a demodulated signal and a known signal

and, furthermore, by the averaging thereof, the phase amount is detected. Document related to claims 6 - 8 of the present application.)

Japanese Unexamined Patent Application No. Heisei 11-103326 (Description of technology in which the correlated value of a signal output from a sampling means is found, and control of the sampling timing is performed.

Document comprising details that are based on cited document 1.)

Japanese Unexamined Patent Application No. Heisei 7-99486 (Description of technology in which a correlation calculation is performed using only the "I" component of the output of the two A/D converters, and control of the sampling timing of the A/D converters is performed.

Prior art technology related to claim 10 of the present application.)

Japanese Unexamined Patent Application No. Heisei 8-111677 (See the description of paragraph 26 in the text. The phase difference is detected by the taking out of the synchronized word from the received signal and the calculation of the correlation thereof with a known synchronized word. Prior art technology that corresponds to the description "...taking out of the known signal from the parallel signals from the symbol detection part 11..." given in the final sentence of paragraph 23 of the specification of the present application.)

Japanese Unexamined Patent Application No. Showa 48-30308
(See the description in claim 1 (a) (b) in the range of
the patent claims of this document. Description of
technology in which two orthogonal carrier waves are
modulated by respectively separate signals "First and
second unique words". A document that comprises details
the same as cited document 5.)